EM02: Advanced Features and Techniques of Embedded Systems Design

EM02: Sistemas Embebidos en FPGA Avanzado

Language: The classes are in Spanish, but working material is in English (available also in English at In-Company).

Who Should Attend? Hardware, firmware, and system design engineers who are interested in deepen Xilinx embedded systems development flow and advanced techniques.

Duration: 24 h (3 days, 8 h/day).

Prerequisites: Knowledge of Essential Embedded Systems Design course (EM02) or equivalent experience with embedded systems design and the Vivado Design Suite. HDL (Verilog or VHDL), C (or C++) programming experience.

Introduction: This course also aids developers understand and utilize advanced components of embedded systems design for architecting a complex system in the Zynq® All Programmable System on a Chip (SoC) or MicroBlaze™ soft processor. Details the individual components in the PS: I/O peripherals, timers, caching, DMA, interrupt, and memory controllers. Emphasis on effective access and usage of the PS DDR controller from PL user logic, efficient PL-to-PS interfacing, and design techniques, tradeoffs, and advantages of implementing functions in the PS or the PL. Introduction to software programing techniques and Linux on Xilinx Embedded System.

Skills Gained: After completing this training, you will know how to:

- Assemble an advanced embedded system
- Take advantage of the various features of Zynq All Programmable SoC and Kintex™ FPGAs, Cortex™-A9 and MicroBlaze processors, including the AXI interconnect and various memory controllers
- Apply advanced debugging techniques, including the use of the Vivado analyzer tool for debugging an embedded processor system and HDL system simulation for processor-based designs
- Identify the steps involved in integrating a memory controller into an embedded system using the Cortex-A9 and MicroBlaze processors
- Integrate an interrupt controller and interrupt handler into an embedded design
- Design a flash memory-based system and boot load from off-chip flash memory.
- Effectively select and design an interface between the Zynq PS and programmable logic (PL) that meets project goals
- Analyze the tradeoffs and advantages of performing a function in software versus PL

Material: Each student will have a computer with the development tools (Vivado 2015.x), documentation, repository whit exercises (and solutions) and a FPGA development board for exercises that require it.

Related Courses:

EM01: Embedded Systems Design with Xilinx FPGA (this course).

EM02: Advanced Features and Techniques of Embedded Systems Design

Other Xilinx Technologies courses:

HL01: HDL Logical Synthesis and Simulation for Xilinx FPGA design

FP01: Essential Vivado Design Suite: 7-Series, TCL, Static Timing Analysis, Constraints.

FP02: Advanced Vivado Design Suite: Advanced Timing, Tools and Techniques.

EML1: Build a Linux distribution for Xilinx FPGA

HLS1: High Level Syntesis for Xilinx FPGAs using Vivado-HLS

DSP1: DSP Design Using System Generator

SDS1: SDSoc development environment

SDA1: SDAccel for algorithm acceleration

Dates, location and registration:

Please visit www.electratraining.org

Price:

EM01: 1650 € Includes cafes and lunches

Course Packs and Discounts:

EM01 + EM02: 2640 € (-20%)
FP01 + FP02: 2640 € (-20%)
HL01 + FP01: 2240 € (-20%)
HL01 + FP01 + FP02: 3340 € (-25%)
HL01+FP01+FP02+EM01+EM02: 4960 € (-36%)
EML1 coming from FP/ EM: 1320 € (-20%)
HLS1 coming from FP/ EM: 1320 € (-20%)

Additional discounts:

Previous ElectraTraining course 5%
Prior Xilinx technology course in last year: 10%
More than one participant from the same company.
It is possible to use Xilinx Training Credits.