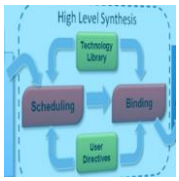

HLS1: High Level Synthesis for Xilinx FPGAs using Vivado-HLS

HLS1: Síntesis de alto nivel para FPGAs de Xilinx con Vivado-HLS

Language: The classes are in Spanish, but working material is in English (available also in English at In-Company).

Who Should Attend? Hardware, firmware, and system design engineers who are interested in use high-level synthesis and accelerate the hardware development process.

Duration: 16 h (2 days, 8 h/day).

Prerequisites: Notions of Digital and Xilinx FPGA design. C, C++ or system-C.

Introduction: Digital design is moving from RTL design levels using HDLs to more productive tool that uses higher level of abstractions. The course introduces the Vivado High-Level Synthesis (HLS) tool. This course covers synthesis strategies, features, improving throughput, area, interface creation, latency, testbench coding, and coding tips. Utilize the Vivado HLS tool to optimize code for high-speed performance in an embedded environment and download for in-circuit validation.

Skills Gained: After completing this training, you will know how to:

- Enhance productivity in HW development by using the Vivado HLS tool
- Know the high-level synthesis flow and how to optimize it.
- Use the Vivado tool HLS for a first project
- Identify the importance of the testbench and use in real case
- Use directives to improve performance and area and select RTL interfaces
- Identify common coding pitfalls as well as methods for improving code for RTL/HW.
- Describe how to use OpenCV functions in the Vivado HLS tool
- Perform system-level integration of IP generated by the Vivado HLS tool

Material: Each student will have a computer with the development tools (Vivado and Vivado-HLS 2015.x), documentation, repository whit exercises (and solutions) and a FPGA development board for exercises that require it.

Related Courses:

EM01: Embedded Systems Design with Xilinx FPGA (this course).

EM02: Advanced Features and Techniques of Embedded Systems Design

SDS1: Embedded SDSoc Development Environment and Methodology

Other Xilinx Technologies courses:

Please visit our web site.

Dates, location and registration:

HLS1 on 24, 25 November. SDS1: 26, 27 November 2015. Visit www.electratraining.org

Price & Course Packs and Discounts:

HLS1: 1150 €
SDS1: 1150 €
HLS1 + SDS1: 2300 -> 1725€ (-25%)
HLS1 + SDS1 coming from Xilimx Embedded Courses (EM01 or EM02): 2300->1610€ (-30%)
HLS1 coming from Xilinx Embedded Courses (EM01 or EM02): 1150 -> 920€ (-20%)
For more than one engineer from same company / institution additional discounts