



## SDS1: Embedded SDSoC Development Environment and Methodology

### SDS1: SDSoC entorno de desarrollo y Metodología

**Language:** The classes are in Spanish, but working material is in English (available also in English at In-Company).

**Who Should Attend?** Hardware, firmware, and system design engineers who are interested in quickly adding hardware acceleration to a software system.

**Duration:** 16 h (2 days, 8 h/day).

**Prerequisites:** Knowledge of Essential Embedded Systems Design course (EM02) or equivalent experience with embedded systems design and the Vivado Design Suite. C/ C++ programming experience. Familiarity with the Vivado Design Suite, notions Vivado-HLS\* tool, and SDK.

**Introduction:** This course is organized to help new designers to the SDSoC development environment to quickly create accelerated systems. The focus is on utilizing the tools to accelerate an existing design at the system architecture level, not on the optimization of the accelerator microarchitectures\*.

\*For the acceleration of microarchitecture is strongly recommended the Vivado-HLS course (HLS1).

**Skills Gained:** After completing this training, you will know how to:

- Identify candidate functions for hardware acceleration by using the TCF profiling tool
- Use the System Debugger's capabilities to control the execution flow.
- Move designated software functions to hardware and estimate the performance of the accelerator and the effect on the entire system

- Override tool defaults to improve the performance of the individual accelerators and the overall system.
- Analyze the tradeoffs and advantages of performing a function in software versus PL
- Effectively select and design an interface between the Zynq PS and programmable logic (PL) that meets project goals

**Material:** Each student will have a computer with the development tools (SDSoC 2015.x), documentation, repository whit exercises (and solutions) and a FPGA development board for exercises that require it.

#### Related Courses:

EM01: Embedded Systems Design with Xilinx FPGA (this course).

EM02: Advanced Features and Techniques of Embedded Systems Design

HLS1: High Level Synthesis for Xilinx FPGAs using Vivado-HLS

#### Other Xilinx Technologies courses:

Please visit our web site.

#### Dates, location and registration:

SDS1: 26, 27 November 2015. HLS1 on 24, 25 November. Visit [www.electratraining.org](http://www.electratraining.org)

#### Price & Course Packs and Discounts:

SDS1: 1150 €      HL01: 1150 €  
HLS1 + SDS1: 2300 -> 1725€ (-25%)  
HLS1 + SDS1 coming from Xilimx Embedded Courses (EM01 or EM02): 2300->1610€ (-30%)  
Additional discounts for several engineers from same company or institution