



## **DL01: HDL (Hardware Description Languages) Logical Synthesis and Simulation for Xilinx FPGA design**

### **DL01: HDL (Lenguajes de descripción HW) Síntesis Lógica y Simulación para FPGAs de Xilinx**

**Language:** The working material is in English, but classes are in Spanish.

**Who Should Attend?** Digital Engineers who want to use VHDL effectively for modeling, design, and synthesis of digital designs.

**Duration:** 24 h (3 days, 8 h/day).

**Prerequisites:** Digital design experience.

**Introduction:** This course is a detailed introduction to the VHDL language. The emphasis is on writing solid synthesizable code and enough simulation code to write a viable testbench. Structural, register transfer level (RTL), and behavioral coding styles are covered. This class addresses targeting Xilinx devices specifically and FPGA devices in general. The information gained can be applied to any digital design by using a top-down synthesis design approach. This course also introduces notions of Verilog and how to interface with VHDL.

**Skills Gained:** After completing this training, you will know how to:

- Implement the VHDL portion of coding for synthesis
- Identify the differences between behavioral and structural coding styles
- Distinguish coding for synthesis versus coding for simulation
- Use scalar and composite data types to represent information

- Use concurrent and sequential control structure to regulate information flow
- Implement common VHDL constructs (Finite State Machines, RAM/ROM data structures)
- Simulate a basic VHDL design
- Write a VHDL testbench and identify simulation-only constructs
- Identify and implement coding best practices
- Optimize VHDL code to target specific silicon resources within the Xilinx FPGA
- Notions of Verilog, and instantiation VHDL-Verilog and vice versa.
- Create and manage designs within the Vivado Design Suite environment

**Material:** Each student will have a computer with the development tools (Vivado 2015.x), documentation, repository with exercises.

#### **Related Courses:**

FP01: Essential Vivado Design Suite

FP02: Advanced Vivado Design Suite

**More Xilinx Courses:** visit our web page

**Dates, location and registration:** Please visit our web page at [www.electratraining.org](http://www.electratraining.org)

**Price:** DL01: 1150 € Includes cafes and lunches

#### **Course Packs and Discounts:**

FP01 + FP02: 2640 € (-20%)

HL01 + FP01: 2240 € (-20%)

HL01 + FP01 + FP02: 3340 € (-25%)