FP01: Essential Vivado Design Suite: Serie-7, TCL, Static Timing Analysis, Design Constraints

FP01: Vivado fundamental: Serie-7, TCL, Análisis estático de tiempos y restricciones de diseño

Language: The working material is in English, but classes are in Spanish (available in English at In-Company)

Who Should Attend? Digital designers who have a working knowledge of HDL (VHDL or Verilog) and who are new to Xilinx FPGAs. Existing Xilinx ISE users who have no previous experience or training with the Xilinx PlanAhead suite and little or no knowledge of 7-series devices. Project managers of FPGA based design.

Duration: 24 h (3 days, 8 h/day).

Prerequisites: Digital design experience. Working HDL knowledge (VHDL or Verilog)

Introduction: This course offers essential training on the Vivado™ software tool flow. Describes main Xilinx device characteristics, Xilinx design constraints (XDC), static timing analysis (STA), good FPGA design practices (instantiate appropriate device resources, use proper HDL coding techniques, make good pin assignments), and how to use Vivado™ unified database. Synthesize, implement, and download a design. Simulate and debug the FPGA system.

Skills Gained:

- Take advantage of the primary 7 series and ultrascale FPGA architectur resources
- Vivado IDE design flows (project based and non-project batch)
- Use the Project Manager, Identify file sets (HDL, XDC, simulation)
- Analyze designs by using the cross-selection capabilities, Schematic viewer, and Hierarchical viewer
- Synthesize, implement and download an HDL design.
- Simulate (XSIM) and debug (Vivado Logic Analyzer) designs
- Analyze reports to a design (utilization, timing, power, etc.)
- Build custom IP with the IP Library utility
- Make basic timing constraints (create_clock, set_input_delay, and set_output_delay)
- Use the essential Tcl-based commands.
- Analyze common STA (Static Timing Report) reports
- Identify synchronous design techniques

Material: Each student will have a computer with the development tools (Vivado 2015.x), documentation, repository whit exercises (and solutions) and a FPGA development boards for exercises that require it.

Related Courses:

HL01: HDL Logical Synthesis and Simulation for Xilinx FPGA design

FP01: Essential Vivado Design Suite: 7-Series, TCL, Static Timing Analysis, Constraints.

FP02: Advanced Vivado Design Suite: Advanced Timing, Tools and Techniques.

Other Xilinx Technologies courses:

EM01: Embedded Systems Design with Xilinx FPGA

EM02: Advanced Features and Techniques of Embedded Systems Design

EML1: Build a Linux distribution for Xilinx FPGA

HLS1: High Level Syntesis for Xilinx FPGAs using Vivado-HLS

DSP1: DSP Design Using System Generator

SDS1: SDSoc development environment

SDA1: SDAccel for algorithm acceleration

Dates, location and registration:

Please visit www.electratraining.org

Price:

FP01: 1650 € Includes cafes and lunches

Course Packs and Discounts:

FP01 + FP02: 2640 € (-20%)
HL01 + FP01: 2240 € (-20%)
HL01 + FP01 + FP02: 3340 € (-25%)
EM01 + EM02: 2640 € (-20%)
HL01+FP01+FP02+EM01+EM02: 4960 € (-36%)
EML1 coming from FP/ EM: 1320 € (-20%)
HLS1 coming from FP/ EM: 1320 € (-20%)

Additional discounts:

Previous ElectraTraining course 5%
Prior Xilinx technology course in last year: 10%
More than one participant from the same company.
It is possible to use Xilinx Training Credits.