FP02: Advanced Vivado Design Suite: Advanced Timing, Tools and Techniques.

FP02: Diseño Vivado FPGAs Avanzado: Timing, herramientas y técnicas

Language: The classes are in Spanish, but working material is in English (available also in English at In-Company).

Who Should Attend? Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity.

Duration: 24 h (3 days, 8 h/day).

Prerequisites: Intermediate knowledge of HDL and FPGA architecture, and experience with the Xilinx Vivado (The knowledge of *FP01: Essential Vivado Design Suite*)

Introduction: This course offers advanced training on the Vivado™ software tool flow. Advanced Timing analysis and Xilinx design constraints (timing exceptions, false paths, and multi-cycle path). Floorplanning techniques to improve design performance and use Tcl scripting in both the project-based and non-project batch design flows. UltraFast design methodology and key areas to optimize designs.

Skills Gained:

- Increase performance by utilizing FPGA design techniques
- Vivado IDE database (DB) objects, Tcl commands for interacting with the DB.
- Apply complete Xilinx design constraints (XDC), including timing exceptions, false paths, and multi-cycle path constraints
- Utilize static timing analysis (STA) to analyze timing results. Pinpoint design bottlenecks by using appropriate timing reports
- Apply advanced I/O timing constraints to meet performance goals
- Describe different synthesis options and how they can improve design performance
- UltraFast design methodology. Identify key areas to optimize your design to meet your design goals and performance objectives
- Optimize HDL code to maximize the FPGA resources that are inferred and meet your performance goals
- Build resets into your system for optimum reliability and design speed
- Use good alternative design practices to improve design reliability (e.g. metastability problems)
- Use Vivado Design Suite reports and utilities to full advantage, especially the Clock Interaction report
- Identify timing closure techniques using the Vivado Design Suite
- Create scripts for the project-based and non-project batch design flows.
- Identify synchronous design techniques

Material: Each student will have a computer with the development tools (Vivado 2015.x), documentation, repository whit exercises (and solutions) and a FPGA development board for exercises that require it.

Related Courses:

HL01: HDL Logical Synthesis and Simulation for Xilinx FPGA design

FP01: Essential Vivado Design Suite: 7-Series, TCL, Static Timing Analysis, Constraints.

FP02: Advanced Vivado Design Suite: Advanced Timing, Tools and Techniques.

Other Xilinx Technologies courses:

EM01: Embedded Systems Design with Xilinx FPGA

EM02: Advanced Features and Techniques of Embedded Systems Design

EML1: Build a Linux distribution for Xilinx FPGA

HLS1: High Level Syntesis for Xilinx FPGAs using Vivado-HLS

DSP1: DSP Design Using System Generator

SDS1: SDSoc development environment

SDA1: SDAccel for algorithm acceleration

Dates, location and registration:

Please visit www.electratraining.org

Price:

FP02: 1650 € Includes cafes and lunches

Course Packs and Discounts:

FP01 + FP02: 2640 € (-20%)
HL01 + FP01: 2240 € (-20%)
HL01 + FP01 + FP02: 3340 € (-25%)
EM01 + EM02: 2640 € (-20%)
HL01+FP01+FP02+EM01+EM02: 4960 € (-36%)
EML1 coming from FP/ EM: 1320 € (-20%)
HLS1 coming from FP/ EM: 1320 € (-20%)

Additional discounts:

Previous ElectraTraining course 5%
Prior Xilinx technology course in last year: 10%
More than one participant from the same company.
It is possible to use Xilinx Training Credits.