FPG02: Advanced Vivado Design Suite: Static Timing Analysis and Xilinx Design Constraints

FPG02: Diseño Vivado FPGAs Avanzado: Análisis estático de tiempos y restricciones de diseño

Language: The classes are in Spanish, but working material is in English (available also in English at In-Company).

Who Should Attend? Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity.

Duration: 16 h (2 days, 8 h/day).

Prerequisites: Intermediate knowledge of HDL and FPGA architecture, and experience with the Xilinx Vivado (The knowledge of *FPG01: Essential Vivado Design Suite*)

Introduction: This course offers detailed training on the Vivado® software tool flow, Xilinx design constraints (XDC), and static timing analysis (STA). Learn to use good FPGA design practices and all FPGA resources to advantage. Learn to fully and appropriately constrain your design by using industry-standard XDC constraints. Learn how the the Vivado IDE design database is structured and learn to traverse the design. Create appropriate timing reports to perform full STA and how to appropriately synthesize your design.

You will also learn the FPGA design best practices and skills to be successful using the Vivado Design Suite. This includes the necessary skills to improve design speed and reliability. This course encapsulates this information with an UltraFast™ design methodology case study. The UltraFast design methodology checklist is also introduced.

Skills Gained:

- Increase performance by utilizing FPGA design techniques
- Vivado IDE database (DB) objects, Tcl commands for interacting with the DB.
- Apply complete Xilinx design constraints (XDC), including timing exceptions, false paths, and multi-cycle path constraints
- Utilize static timing analysis (STA) to analyze timing results. Pinpoint design bottlenecks by using appropriate timing reports
- Apply advanced I/O timing constraints to meet performance goals
- Describe different synthesis options and how they can improve design performance
- UltraFast design methodology. Identify key areas to optimize your design to meet your design goals and performance objectives
- Optimize HDL code to maximize the FPGA resources that are inferred and meet your performance goals
- Build resets into your system for optimum reliability and design speed
- Use good alternative design practices to improve design reliability (e.g. metastability problems)
- Use Vivado Design Suite reports and utilities to full advantage, especially the Clock Interaction report
- Identify timing closure techniques using the Vivado Design Suite
- Create scripts for the project-based and non-project batch design flows.
- Identify synchronous design techniques

Material: Each student will have a computer with the development tools (Vivado 2016.x), documentation, repository whit exercises (and

solutions) and a FPGA development board for exercises that require it.

Related Courses:

HDL01: VHDL (HW Description Language) Logical Synthesis and Simulation for Xilinx FPGA design

FPG01: Essential Vivado Design Suite: 7-Series, UltraScale, US+, TCL, Static Timing Analysis, Constraints.

FPG03: Advanced Vivado Design Suite: Advanced Tools and Techniques

Other Xilinx Technologies courses:

EM01: Embedded Systems Design with Xilinx FPGA
EM02: Advanced Features and Techniques of Embedded Systems Design
EML1: Build a Linux distribution for Xilinx FPGA
HLS1: High Level Syntesis using Vivado-HLS
SDS1: SDSoc development environment

Dates, location and registration:

Please visit www.electratraining.org

Price:

FPG02: 960 € Includes cafes and lunches

Course Packs:

FPG01 + FPG02: 1440 € (-20%)
FPG02 + FPG03: 1520 € (-21%)
HDL01 + FPG01 + FPG02: 1880 € (-25%)
FPG01 + FPG02 + FPG03: 2070 € (-25%)
HDL01+FPG01+FPG02+FPG03: 2580 € (-25%)

Additional discounts:

Previous ElectraTraining course 5%
Prior Xilinx technology course in last year: 10%
More than one participant from the same company.
It is possible to use Xilinx Training Credits.