FPG03: Advanced Vivado Design Suite: Advanced Tools and Techniques

FPG03: Diseño Vivado FPGAs Avanzado: herramientas y técnicas avanzadas

Language: The classes are in Spanish, but working material is in English (available also in English at In-Company).

Who Should Attend? Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity.

Duration: 16 h (2 days, 8 h/day).

Prerequisites: knowledge of HDL and FPGA architecture, and experience with the Xilinx Vivado (The knowledge of *FPG01 and FPG02: Essential Vivado Design Suite, STA and Constrainsts*)

Introduction: This course tackles the most sophisticated aspects of the Vivado® Design Suite and Xilinx hardware. Learn to utilize advanced static timing analysis and apply timing constraints for source- synchronous and system-synchronous inter-faces. Utilize floorplanning techniques to improve design performance and use Tcl scripting in both the project-based and non-project batch design flows.

Skills Gained:

- Increase performance by utilizing FPGA design techniques
- Explain the impact that manufacturing process variations have on timing analysis
- Describe how min/max timing analysis information is conveyed in a timing report
- Utilize the custom timing report options to build optimal timing reports
- Utilize some of the advanced timing report features to control how delay paths are displayed in timing reports
- Make appropriate I/O timing constraints and design modifications for source-synchronous and system-synchronous interfaces
- Analyze a timing report to identify how to center the clock in the data eye
- Utilize the most advanced features (area constraints) of the Vivado IDE to improve design performance
- Use the Hierarchical viewer, Schematic viewer, and timing report information to make the best area constraints
- Use scripting in project-based and non-project batch flows to synthesize, implement, and generate custom timing reports
- Describe different synthesis options and how they can improve design performance
- UltraFast design methodology. Identify key areas to optimize your design to meet your design goals and performance objectives
- Optimize HDL code to maximize the FPGA resources that are inferred and meet your performance goals

Material: Each student will have a computer with the development tools (Vivado 2016.x), documentation, repository whit exercises (and solutions) and a FPGA development board for exercises that require it.

Related Courses:

HDL01: VHDL (HW Description Language) Logical Synthesis and Simulation for Xilinx FPGA design

FPG01: Essential Vivado Design Suite: 7-Series, UltraScale, US+, TCL, Static Timing Analysis, Constraints.

FPG02: Advanced Vivado Design Suite: Static Timing Analysis and Xilinx Design Constraints

Other Xilinx Technologies courses:

EM01: Embedded Systems Design with Xilinx FPGA

EM02: Advanced Features and Techniques of Embedded Systems Design
EML1: Build a Linux distribution for Xilinx FPGA
HLS1: High Level Syntesis using Vivado-HLS
DSP1: DSP Design Using System Generator
SDS1: SDSoc development environment

Dates, location and registration:

Please visit www.electratraining.org

Price:

FPG03: 960 € Includes cafes and lunches

Course Packs:

FPG02 + FPG03: 1520 € (-21%)
FPG01 + FPG02 + FPG03: 2070 € (-25%)
HDL01+FPG01+FPG02+FPG03: 2580 € (-25%)

Additional discounts:

Previous ElectraTraining course 5%
Prior Xilinx technology course in last year: 10%
More than one participant from the same company.
It is possible to use Xilinx Training Credits.