HDL01: HDL (Hardware Description Languages) Logical Synthesis and Simulation for Xilinx FPGA design

HDL01: HDL (Lenguajes de descripción HW) Síntesis Lógica y Simulación para FPGAs de Xilinx

Language: The working material is in English, but classes are in Spanish.

Who Should Attend? Digital Engineers who want to use VHDL effectively for modeling, design, and synthesis of digital designs.

Duration: 16 h (2 days, 8 h/day).

Prerequisites: Digital design experience.

Introduction: This course is a detailed introduction to the VHDL language. The emphasis is on writing solid synthesizable code and enough simulation code to write a viable testbench. Structural, register transfer level (RTL), and behavioral coding styles are covered. This class addresses targeting Xilinx devices specifically and FPGA devices in general. The information gained can be applied to any digital design by using a top-down synthesis design approach. This course also introduce notions of Verilog and how to interface with VHDL.

Skills Gained: After completing this training, you will know how to:

- Implement the VHDL portion of coding for synthesis
- Identify the differences between behavioral and structural coding styles
- Distinguish coding for synthesis versus coding for simulation
- Use scalar and composite data types to represent information
- Use concurrent and sequential control structure to regulate information flow
- Implement common VHDL constructs (Finite State Machines, RAM/ROM data structures)
- Simulate a basic VHDL design
- Write a VHDL testbench and identify simulation-only constructs
- Identify and implement coding best practices
- Optimize VHDL code to target specific silicon resources within the Xilinx FPGA
- Notions of Verilog, and instantiation VHDL-Verilog and vice versa.
- Create and manage designs within the Vivado Design Suite environment

Material: Each student will have a computer with the development tools (Vivado 2016.x), documentation, repository whit exercises.

Related Courses:

FPG01: Essential Vivado Design Suite: 7-Series, UltraScale, US+, TCL, Static Timing Analysis, Constraints.

Other Xilinx Technologies courses:

FPG02: Advanced Vivado Design Suite: Static Timing Analysis and Xilinx Design Constraints
FPG03: Advanced Vivado Design Suite: Advanced Tools and Techniques
EM01: Embedded Systems Design with Xilinx FPGA
EM02: Advanced Features and Techniques of Embedded Systems Design
EML1: Build a Linux distribution for Xilinx FPGA
HLS1: High Level Syntesis using Vivado-HLS
SDS1: SDSoc development environment

Price:

HDL01: 680 € Includes cafes and lunches

Course Packs:

HDL01 + FPG01: 1250 (-18%)
HDL01 + FPG01 + FPG02: 1880 € (-25%)
HDL01 + FPG01 + FPG03: 1880 € (-25%)
HDL01+FPG01+FPG02+FPG03: 2580 € (-25%)

Dates, location and registration: Please visit our web page at www.electratraining.org

Additional discounts:

Previous ElectraTraining course 5%
Prior Xilinx technology course in last year: 10%
More than one participant from the same company.
It is possible to use Xilinx Training Credits.