VRLG01: Designing with Verilog. Logical Synthesis and Simulation for Xilinx FPGA design

VRLG01: Diseñando con Verilog. Síntesis Lógica y Simulación para FPGAs de Xilinx

Language: The working material is in English, but classes are in Spanish.

Who Should Attend? Digital Engineers who want to use VHDL effectively for modeling, design, and synthesis of digital designs.

Duration: 24 h (3 days, 8 h/day).

Prerequisites: Digital design experience.

Introduction: This comprehensive course is a thorough introduction to the Verilog language. The emphasis is on writing Register Transfer Level (RTL) and behavioral source code. This class addresses targeting Xilinx devices specifically and FPGA devices in general. The information gained can be applied to any digital design by using a top-down synthesis design approach. This course combines insightful lectures with practical lab exercises to reinforce key concepts. You will also learn advanced coding techniques that will increase your overall Verilog proficiency and enhance your FPGA optimization. This course covers Verilog 1995 and 2001.

In this three-day course, you will gain valuable hands-on experience. Incoming students with little or no Verilog knowledge will finish this course empowered with the ability to write efficient hardware designs and perform high-level HDL simulations.

The labs for this course provide a practical foundation for creating synthesizable RTL code. All aspects of the design flow are covered in the labs. The labs are written, synthesized, behaviorally simulated, and implemented by the student. The focus of the labs is to write code that will optimally infer reliable and high-performance circuits. The labs culminate in a functional calculator that students verify in simulation.

Skills Gained: After completing this training, you will know how to:

- Write RTL Verilog code for synthesis
- Write Verilog test fixtures for simulation
- Create a Finite State Machine (FSM) by using Verilog
- Target and optimize Xilinx FPGAs by using Verilog
- Use enhanced Verilog file I/O capability
- Run a timing simulation by using Xilinx Simprim libraries
- Notions of VHDL, and instantiation VHDL-Verilog and vice versa.
- Create and manage designs within the Vivado Design Suite environment
- Download to the evaluation demo board

Material: Each student will have a computer with the development tools (Vivado 2017.x), documentation, repository whit exercises.

Related Courses:

FPGA01: Diseño FPGA de Xilinx usando Vivado Design Suite I (Vivado Fundamental)

VHDL01: Designing with VHDL. Logical Synthesis and Simulation for Xilinx FPGA design

Other Xilinx Technologies courses:

FPGA02: Diseño FPGA de Xilinx usando Vivado Design Suite 2 (Vivado Avanzado II)
FPGA03: Diseño FPGA de Xilinx usando Vivado Design Suite 3 (Vivado Avanzado III)
FPGA04: Diseño FPGA de Xilinx usando Vivado Design Suite 4 (Vivado Avanzado IV)
EMB01: Esencial Sistemas Embebidos en FPGA de Xilinx
EMB02: Sistemas Embebidos en FPGA Avanzado
EML1: Construir una distribución Linux para FPGAs de Xilinx
EMB11: Zynq UltraScale+ MPSoC para arquitectos de sistemas
HLS01: Síntesis de alto nivel para FPGAs de Xilinx con Vivado-HLS
SDS01: Diseño de sistemas con Xilinx SDSoc
SDA02: Uso del framework OpenCL para FPGAs (Entorno de desarrollo SDAccel)

Price:

VRG01: 990 € Includes cafes and lunches

Course Packs:

VRG01 + FPGA01: 1480 (-19%)
VRG01 + FPGA01 + FPGA02: 2090 € (-25%)
VRG01 + FPGA01 + FPGA02 + FPGA03: 2775 € (-26%)

Dates, location and registration: Please visit our web page at www.electratraining.org

Additional discounts:

Previous ElectraTraining course 5%
Prior Xilinx technology course in last year: 10%
More than one participant from the same company.
It is possible to use Xilinx Training Credits.