



EMB02: Advanced Features and Techniques of Embedded Systems Design

EMB02: Sistemas Embebidos en FPGA Avanzado

Language: The classes are in Spanish, but working material is in English (available also in English at In-Company).

Who Should Attend? Hardware, firmware, and system design engineers who are interested in deepening Xilinx embedded systems development flow and advanced techniques.

Duration: 16 h (2 days, 8 h/day).

Prerequisites: Knowledge of Essential Embedded Systems Design course (EMB01) or equivalent experience with embedded systems design and the Vivado Design Suite. HDL (Verilog or VHDL), C (or C++) programming experience.

Introduction: This course also aids developers understand and utilize advanced components of embedded systems design for architecting a complex system in the Zynq® All Programmable System on a Chip (SoC) or MicroBlaze™ soft processor. Details the individual components in the PS: I/O peripherals, timers, caching, DMA, interrupt, and memory controllers. Emphasis on effective access and usage of the PS DDR controller from PL user logic, efficient PL-to-PS interfacing, and design techniques, tradeoffs, and advantages of implementing functions in the PS or the PL. Introduction to software programming techniques and Linux on Xilinx Embedded System.

Skills Gained: After completing this training, you will know how to:

- Assemble an advanced embedded system
- Take advantage of the various features of Zynq All Programmable SoC and Kintex™ FPGAs, Cortex™-A9 and MicroBlaze

processors, including the AXI interconnect and various memory controllers

- Apply advanced debugging techniques, including the use of the Vivado analyzer tool for debugging an embedded processor system and HDL system simulation for processor-based designs
- Identify the steps involved in integrating a memory controller into an embedded system using the Cortex-A9 and MicroBlaze processors
- Integrate an interrupt controller and interrupt handler into an embedded design
- Design a flash memory-based system and boot load from off-chip flash memory.
- Effectively select and design an interface between the Zynq PS and programmable logic (PL) that meets project goals
- Analyze the tradeoffs and advantages of performing a function in software versus PL

Material: Each student will have a computer with the development tools (Vivado 2017.x), documentation, repository with exercises (and solutions) and a FPGA development board for exercises that require it.

Related Courses:

EMB01: Embedded Systems Design with Xilinx FPGA.

FPGA01: Diseño FPGA de Xilinx usando Vivado Design Suite 1 (Vivado Fundamental)

FPGA02: Diseño FPGA de Xilinx usando Vivado Design Suite 2 (Vivado Avanzado II)

FPGA03: Diseño FPGA de Xilinx usando Vivado Design Suite 3 (Vivado Avanzado III)

FPGA04: Diseño FPGA de Xilinx usando Vivado Design Suite 4 (Vivado Avanzado IV)

Other Xilinx Technologies courses:



EMLX1: Linux en FPGAs de Xilinx: Diseño Linux
Empotrado con PetaLinux

CONNI: Conectividad en Xilinx FPGA:
Designing with Serial Transceivers

VRLG01: Designing with Verilog. Logical
Synthesis and Simulation for Xilinx
FPGA design

EMB11: Zynq UltraScale+ MPSoC para
arquitectos de sistemas

HLS01: Síntesis de alto nivel para FPGAs de
Xilinx con Vivado-HLS

SDS01: Diseño de sistemas empotrados con
Xilinx SDSoc

Dates, location and registration:

Please visit www.electratraining.org

Price:

EMB02: 980 € Includes cafes and lunches

Course Packs and Discounts:

EMB01 + EMB02: 1560 € (-20%)

FPGA03 + FPG0A4: 1520 € (-21%)

FPGA02 + FPGA03 + FPGA04: 2160 € (-25%)

FPGA01 + FPGA02 + FPGA03 + FPGA04:
2680 € (-28%)

VHDL01 + FPGA01 + FPGA02 + FPGA03 +
FPGA04: 3300 € (-30%)

HLS1 + SDS1: 1550€ (-20%)

HLS1 + SDS1 coming from Xilinx Embedded
Courses (EM01 or EM02): 1445€ (-25%)

HLS1 o SDS1 coming from Xilinx Courses
(EMB01, EMB02, FPGA1, FPGA2, FPGA3 or
FPGA4): 790€ (-18%)

Additional discounts:

Previous ElectraTraining course 5%

Prior Xilinx technology course in last year: 10%

Several participant from the same company.

It is possible to use Xilinx Training Credits.