FPGA04: Designing FPGAs using Vivado Design Suite 4 (Advanced Vivado IV)

FPGA04: Diseño FPGA Xilinx usando Vivado Design Suite 4 (Vivado Avanzado IV)

Language: The classes are in Spanish, but working material is in English (available also in English at In-Company).

Who Should Attend? Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity.

Duration: 16 h (2 days, 8 h/day).

Prerequisites: knowledge of HDL and FPGA architecture, at least six month experience with the Xilinx Vivado (The knowledge of *FPGA01, FPGA02 and FPGA03 are recommended*)

Introduction: This course tackles the most sophisticated aspects of the Vivado® Design Suite and Xilinx hardware. This course enables you to use the advanced capabilities of the Vivado Design Suite to achieve design closure.

Skills Gained:

- Apply appropriate I/O timing constraints and design modifications for source-synchronous and system-synchronous interfaces
- Analyze a timing report to identify how to center the clock in the data eye
- Use Tcl scripting in non-project batch flows to synthesize, implement, and generate custom timing reports
- Utilize floorplanning techniques to improve design performance
- Employ advanced implementation options, such as incremental compile flow, physical optimization techniques, and re-entrant mode as last mile strategies
- Utilize Xilinx security features, bitstream encryption, and authentication using AES for design and IP security
- Identify advanced FPGA configurations, such as daisy chains and gangs, for configuring multiple FPGAs in a design
- Debug a design at the device startup phase to debug issues related to startup events, such as MMCM lock and design coming out of reset

Material: Each student will have a computer with the development tools (Vivado 2017.x), documentation, repository whit exercises (and solutions) and a FPGA development board for exercises that require it.

Related Courses:

VHDL01: Designing with VHDL. Logical Synthesis and Simulation for Xilinx FPGA design
FPGA01: Diseño FPGA de Xilinx usando Vivado Design Suite 1 (Vivado Fundamental)
FPGA02: Diseño FPGA de Xilinx usando Vivado Design Suite 2 (Vivado Avanzado II)
FPGA03: Diseño FPGA de Xilinx usando Vivado Design Suite 3 (Vivado Avanzado III)

Other Xilinx Technologies courses:

EMB01: Esencial Sistemas Embebidos en FPGA de Xilinx
EMB02: Sistemas Embebidos en FPGA Avanzado
EMLX1: Linux en FPGAs de Xilinx: Diseño Linux Empotrado con PetaLinux
CONN1: Conectividad en Xilinx FPGA: Designing with Serial Transceivers
VRLG01: Designing with Verilog. Logical Synthesis and Simulation for Xilinx FPGA design
EMB11: Zynq UltraScale+ MPSoC para arquitectos de sistemas

HLS01: Síntesis de alto nivel para FPGAs de Xilinx con Vivado-HLS
SDS01: Diseño de sistemas con Xilinx SDSoc
SDA02: Uso del framework OpenCL para FPGAs (SDAccel)

Dates, location and registration:

Please visit www.electratraining.org

Price:

FPGA04: 960 € Includes cafes and lunches

Course Packs:

FPGA03 + FPG0A4: 1520 € (-21%)
FPGA02 + FPGA03 + FPGA04: 2160 € (-25%)
FPGA01 + FPGA02 + FPGA03 + FPGA04: 2680 € (-28%)
VHDL01 + FPGA01 + FPGA02 + FPGA03 + FPGA04: 3300 € (-30%)

Additional discounts:

Previous ElectraTraining course 5%
Prior Xilinx technology course in last year: 10%
More than one participant from the same company.
It is possible to use Xilinx Training Credits