Versal-HLS. High-Level Synthesis (HLS) for Embedded Heterogeneous Design

Síntesis de alto nivel (HLS) para el diseño de sistemas empotrados heterogéneos (Versal-HLS)

Course Description

High-Level Synthesis (HLS) plays a transformative role in digital design, particularly in the context of FPGA and SoC development. HLS bridges the gap between software and hardware design, improving productivity, enabling rapid innovation, and making hardware acceleration accessible to a wider audience (including those without deep HDL experience). This training provides a thorough introduction to high-level synthesis using the AMD Vitis™ Unified IDE (former known as Vivado-HLS and then Vitis-HLS). Additionally we will show illustrates the tool flow for developing HLS and AI Engine components as well as integrating an entire system project when designing an embedded heterogeneous system using the v++ tools and AMD Vitis™ Unified IDE.

The focus of this course is on:

- Converting C/C++ designs into RTL implementations
- Learning the HLS component development flow
- Creating I/O interfaces for designs
- Applying different optimization techniques to designs
- Improving throughput, area, latency, and logic by using different HLS pragmas/directives
- Exporting IP that can be used with the Vivado™ IP catalog
- Migrating designs from the classic Vitis HLS tool to the Vitis Unified IDE
- Describing an embedded heterogeneous system design
- Developing HLS and AIE components using the AMD Vitis tool
- Utilizing the v++ command line tools for component compilation, linking, and packaging to run emulation
- Demonstrating the system design flow for a heterogeneous embedded system using the AMD Vitis Unified IDE

Language: The classes are in Spanish, but working material is in English (available English at In-Company).

Who Should Attend? Software and hardware developers, system architects, and anyone who needs to accelerate their software applications using AMD devices. HDL (Verilog – VHDL) designers seeking to enhance productivity through the adoption of high-level synthesis techniques.

Prerequisites

- Comfort with the C/C++ programming language
- Familiarity with AMD FPGAs and SoCs
- Basic experience with Vitis™ AMD Vitis tool flow

Tools and Hardware:

- Software Tools: Vivado Design Suite, Vitis Unified IDE, Petalinux (version 2025.1)
- Hardware: AMD Adaptive SoC (mainly Versal but also MPSoC/RFSoC)

Course Outline:

The training is structured over three consecutive days, comprising 24 hours of instruction, with approximately half of the time dedicated to hands-on lab sessions.

- HLS overview and development flow
- Parallel programming and I/O protocols (block/port-level, AXI)
- Using the Vitis command-line tools and code analyzer
- Interface and protocol design (AXI4, AXI4-Lite, AXI4-Stream)
- Labs on interface design and command-line synthesis
- Optimization techniques: PIPELINE, DATAFLOW, array handling
- Tuning for latency, area, and AXI system performance
- Use of HLS libraries and arbitrary precision types
- Pointer usage and limitations
- Full system integration and Vivado IP export
- Migration strategies from legacy Vitis HLS
- Application Mapping & Partitioning – Mapping computation models to SoC domains
- Using the Vitis Unified IDE – Terminology, application flow
- Tool Flow for Heterogeneous Systems – Toolchain mapping, image assembly
- Design Report Analysis – Using IDE reports for performance/debug
- AI Engine Debug & Trace – Emulation and in-application debugging
- v++ Command Line Tools – Compile/link/ package kernels
- Custom Platform Development – Using Vivado, RTL, HLS, and Vitis
- System Design Flow – Integrating AI Engine, HLS, and RTL kernels into full systems

Related Courses:

- Versal-ADM: Designing with the Versal Adaptive SoC: Architecture and Design Methodology
- Versal-AIE. Designing with Versal AI Engine: Architecture and Design Flow

Other Xilinx Technologies courses:

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Dates, location and registration:

Visit https://electratraining.org/

Prices and Discounts:

- Versal-ADM: 2580€
- Versal-HLS: 1980€
- Versal-AIE: 2070€
- ADM + HLS: 3920€ (-14%)
- ADM + AIE: 3990€ (-14%)
- ADM + HLS + AIE: 5500 (-17%)

For more than one engineer from same company / institution additional discounts.