Versal-AIE. Designing with Versal AI Engine: Architecture and Design Flow

Diseñando con los AI Engine de Versal: Arquitectura y flujo de diseño (Versal-AIE)

Course Description

The Versal™ AI Engines (from AMD-Xilinx) are a central innovation within the Versal Adaptive SoC family, designed to provide high-performance, energy-efficient compute capabilities for AI, signal processing, and data-intensive applications. This course describes the AMD Versal™ AI Engine architecture, the data communications within an AI Engine array and between the PL and AI Engines, how to program the AI Engines (single kernel programming and multiple kernel programming using data flow graphs), and how to analyze a kernel program by using various debugger features. Developing AI Engine DSP designs using AMD Vitis™ Model Composer is also demonstrated. In addition, advanced features in adaptive data flow (ADF) graph implementation, such as using streams, cascade streams, buffer location constraints, runtime parameterization, and APIs to update and read runtime parameters, are covered.

The emphasis of this course is on:

- Describing the AI Engine (AIE) architecture
- Illustrating the Versal AI Engine tool flow
- Designing with single AI Engine kernels and analyzing the performance of scalar and vectorized kernels using the Vitis™ unified software platform
- Designing with multiple AI Engine kernels using data flow graphs with the Vitis Unified IDE
- Reviewing the data movement between AI Engines, between AI Engines via memory and DMA, and between AI Engines to programmable logic (PL)
- Analyzing and debugging kernel performance
- Describing the AIE-ML architecture
- Illustrating the programming model for the AIE-ML
- Implementing a system-level design flow (PS + PL + AIE) and the supported simulation
- Using an interface for data movement between the PL and AI Engine
- Utilizing AI Engine APIs for arithmetic operations and advanced functions to implement filters
- Utilizing the AI Engine DSP library for faster development
- Applying runtime parameters for an AI Engine design
- Utilizing the Vitis Model Composer tool for AI Engine designs
- Analyzing reports using the Analysis view of the Vitis Unified IDE

Language: The classes are in Spanish, but working material is in English (available English at In-Company).

Who Should Attend? – Software and hardware developers, system architects, and anyone who needs to accelerate their software applications using AMD Versal devices

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enhance productivity through the adoption of high-level synthesis techniques.

Prerequisites

- Comfort with the C/C++ programming language
- Basic understanding of signal processing principles
- Familiarity with AMD FPGAs and SoCs
- Basic experience with Vitis™ AMD Vitis tool flow

Tools and Hardware:

- Software Tools: Vivado Design Suite, Vitis Unified IDE (version 2025.1)
- Hardware: AMD Versal Adaptive SoC

Course Outline:

The training is structured over three consecutive days, comprising 24 hours of instruction, with approximately half of the time dedicated to hands-on lab sessions.

- AI Engine Architecture & Interfaces – Memory, AXI-Stream, cascade, locks
- Memory & Data Movement – Inter-tile communication, DMA, array access
- Application Mapping & Partitioning – Functional models mapped to compute domains
- Tool Flow Introduction – Vitis platform build and compile process
- Programming with Scalar & Vector Types – SIMD registers, vector APIs
- AI Engine APIs & I/O Buffers – Streaming APIs, data movement techniques
- Analyzing AI Engine Reports – Performance and resource usage visualization
- Single Kernel Programming – Scalar and vector-based implementation
- Adaptive Data Flow (ADF) Graphs – Multi-kernel integration and runtime control
- AI Engine-ML Architecture – Advanced tile and memory structures for ML
- Programming AIE-ML – Shared and external buffer usage, graph modeling
- Design Report Analysis – Debug and optimization via Vitis Analyzer
- Use of AI Engine arithmetic APIs and intrinsics for DSP/filtering
- System-level flow and Vitis-to-Vivado export
- Vitis Model Composer – DSP design using graphical tools

Related Courses:

- Versal-HLS. High-Level Synthesis (HLS) for Embedded Heterogeneous Design
- Versal-ADM: Designing with the Versal Adaptive SoC: Architecture and Design Methodology

Other Xilinx Technologies courses:

Please visit our web site.

Dates, location and registration:

Visit https://electratraining.org/

Prices and Discounts:

- Versal-ADM: 2580€
- Versal-HLS: 1980€
- Versal-AIE: 2070€
- ADM + HLS: 3920€ (-14%)
- ADM + AIE: 3990€ (-14%)
- ADM + HLS + AIE: 5500 (-17%)

For more than one engineer from same company / institution additional discounts.