/INVITATION AMD

INVINET SILICA



Join Avnet Silica for the AMD Embedded Tour in Madrid, a one-day event connecting embedded designers with AMD experts, strategic partners, and industry peers. Whether you're building smarter systems, accelerating AI at the edge, or optimising compute architectures, this is your opportunity to streamline your development and make better design decisions - faster.

TACKLE KEY CHALLENGES LIKE:

- · Integrating compute and acceleration without added complexity
- · Maximising edge performance within tight power budgets
- · Working with toolchains that don't always fit your needs

Choose from two tracks and explore how the AMD embedded portfolio - x86, FPGA, adaptive SoCs, and scalable tools - enables unmatched system-level efficiency and design freedom across real-world workloads. We'll also be joined by our partner Advantech for a deepdive into how they're innovating with AMD x86 solutions.

You'll also have the opportunity to meet with some of our supplier partners during the marketplace and get hands-on with cutting-edge embedded technologies. You can find the full list of the partners on the registration page.

Find agenda on the next page >>

SEATS ARE LIMITED - RESERVE YOURS NOW.

Featuring our partner:



DATE:

17th June 2025

LOCATION:

Covarrubias The One Sala White Calle de Covarrubias, 1 28010, Madrid

CONTACT:

Belen.Matilla@avnet.eu



AGENDA:

08:30 - 09:30	Arrival and Registration Grab your badge, coffee, and head on over to our Marketplace.	
09:30 - 10:00	Welcome and Opening Remarks Setting the stage for a day of innovation, insight, and engineering excellence. Belén Matilla, Avnet Silica and Alberto Fusaschi, AMD	
10:00 – 11:00	AMD Embedded Portfolio - FPGAs, adaptive SoCs and x86 CPUs Overview of the AMD Embedded portfolio including the newest FPGA, adaptive SoCs families, Embedded x86 CPUs and the Al and software solutions. Thilo Ohlemueller, AMD	
11:00 - 12:00	AMD: The Performant, Predictable and Proven Choice Discover why AMD FPGAs and adaptive SoCs are the Performant, Predictable and Proven choice. Thilo Ohlemueller, AMD	
12:00 - 12:30	Coffee Break	
	Track 1	Track 2
12:30 - 13:30	AMD Cost Optimised Portfolio Gain the insights and expertise to confidently choose the right AMD cost-optimised solution for your design. Thilo Ohlemueller, AMD	Why Choose AMD Embedded x86 Options and tools for building x86 based embedded solutions and illustration of the Embedded product support flow. Mani Anandan, AMD
13:30 - 14:30	Introduction to Versal AIE for DSP Expand your AI Engines architecture knowledge with an in-depth overview of the development cycle and methodology. Marco Escajadillo Calizaya, AMD	Partnering for Success: x86 ODM Perspectives Hear how AMD ODM partner Advantech are innovating with AMD x86 solutions. TBC, Advantech
14:30 - 15:30	Lunch and Marketplace Explore live demos, meet AMD partners, and discuss real-world use cases with peers and experts.	
15:30 - 16:30	Multi Gigabit Links Optimisation and Troubleshooting using IBERT Explore the key features of Error Ratio Tester (IBERT) and how to develop a strategy to optimise link performance. Francesco Contu, Avnet Silica	Implementing DSP algorithms in FPGA Compare FPGA implementation methods for DSP with practical examples using various tools, including HDL with cocotb, Vitis HLS, Vitis Model Composer, and Matlab HDL Coder. Sergio López Buedo, Electratraining
16:30 - 17:30	Versal RF and Versal Gen2 Discover the cutting-edge solutions with latest AMD technologies tailored for Space, Defence and high performance industrial applications. Francesco Contu, Avnet Silica	Secure Boot, TPM and LUKS Flash Encryption Enhance the security of your AMD Zynq/ZynqUS+/ Versal based products using state of the art encryption technologies and experience a live demo of AMD KV260 Eval Kit. Marco Hoefle, Avnet Silica
17:30 - 17:45	Wrap-Up, Takeaways & Raffle Key insights from the day - plus a chance to win some cool prizes in our raffle!	